CLAIMS

What is claimed is:

1. A computer system comprising:

a cache memory having a plurality of cache lines each of which stores data;

a storage area to store a data operand; and

an execution unit coupled to said storage area to operate on data elements in said data operand to invalidate data in a predetermined portion of the plurality of cache lines in response to receiving a single instruction.

2. The computer system of Claim 1, wherein the data operand is a register location.

3. The computer system of Claim 2, wherein the register location contains a portion of a starting address of the cache line in which data is to be invalidated.

4. The computer system of Claim 3, wherein the portion of the starting address includes a plurality of most significant bits of the starting address.

5. The computer system of Claim 4, wherein execution unit shifts the data elements by a predetermined number of bit positions to obtain the starting address of the cache line in which data is to be invalidated.

6. The computer system of Claim 1, wherein the predetermined portion of the plurality of cache lines is a page in the cache memory.

7. A computer system comprising:

a first storage area to store data;

a cache memory having a plurality of cache lines each of which stores data;

a second storage area to store a data operand; and

an execution unit coupled to said first storage area, said second storage area, and said cache memory, said execution unit to operate on data elements in said data operand to copy data from a predetermined portion of the plurality of cache lines in the cache memory to the first storage area, in response to receiving a single instruction.

8. The computer system of Claim 7, wherein the data operand is a register location.

9. The computer system of Claim 8, wherein the register location contains a plurality of most significant bits of a starting address of the cache line in which data is to be copied.

10. The computer system of Claim 9, wherein execution unit shifts the data elements by a predetermined number of bit positions to obtain the starting address of the cache line in which data is to be copied.

11. The computer system of Claim 7, wherein the predetermined portion of the plurality of cache lines is a page in the cache memory.

12. The computer system of Claim 7, wherein the execution unit further invalidates data in the predetermined portion of the plurality of cache lines in response to receiving the single instruction, upon copying the data to the first storage area.

13 A processor comprising:

a decoder configured to decode instructions, and

a circuit coupled to said decoder, said circuit in response to a single decoded instruction being configured to:

obtain a starting address of a predetermined area of a cache memory on which the instruction will be performed;

invalidate data in the predetermined area of cache memory.

14. The processor of Claim 13, wherein a portion of the starting address is located in a register specified in the decoded instruction.

15. The processor of Claim 13, wherein the portion of the starting address includes a plurality of most significant bits of the starting address.

16. The processor of Claim 15, wherein the circuit shifts the data elements by a predetermined number of bit positions to obtain the starting address of the cache line in which data is to be invalidated.

17. The processor of Claim 13, wherein the predetermined portion of the plurality of cache lines is a page in the cache memory.

18. A processor comprising:

a decoder configured to decode instructions, and

a circuit coupled to said decoder, said circuit in response to a single decoded instruction being configured to:

obtain a starting address of a predetermined area of a cache memory on which the instruction will be performed;

copy data in the predetermined area of cache memory;

store the copied data in a storage area separate from the cache memory.

19. The processor of Claim 18, wherein a portion of the starting address is located in a register specified in the decoded instruction.

20. The processor of Claim 18, wherein the portion of the starting address includes a plurality of most significant bits of the starting address.

21. The processor of Claim 20, wherein the circuit shifts the data elements by a predetermined number of bit positions to obtain the starting address of the cache line in which data is to be copied.

22. The processor of Claim 20, wherein the predetermined portion of the plurality of cache lines is a page in the cache memory.

23. The processor of Claim 20, wherein said circuit further invalidates the data in the predetermined portion of the plurality of cache lines in response to receiving the single instruction, upon copying the data to the storage area.

24. A computer-implemented method, comprising:

a) decoding a single instruction;

b) in response to said step of decoding the single instruction, obtaining a starting address of a predetermined area of a cache memory on which the single instruction will be performed; and

c) completing execution of said single instruction by invalidating data in the predetermined area of cache memory.

25. The method of Claim 24, wherein c) comprises setting an invalid bit corresponding to the predetermined area of cache memory.

26. The method of Claim 24, wherein b) comprises:

b.1) obtaining a portion of the starting address from a storage location specified in the decoded instruction;

b.2) shifting the portion of the starting address by a predetermined number of bit positions to obtain the starting address of the cache line in which data is to be invalidated.

27. The method of Claim 26, wherein in b.1) the portion of the starting address contains a plurality of most significant bits of the starting address, and

wherein in b.2), the predetermined number of bit positions represent the number of least significant bits of the starting address.

28. The method of Claim 24, wherein the predetermined portion of the plurality of cache lines is a page in the cache memory.

29. A computer-implemented method, comprising:

a) decoding a single instruction;

b) in response to said step of decoding the single instruction, obtaining a starting address of a predetermined area of a cache memory on which the single instruction will be performed; and

c) completing execution of said single instruction by copying data in the predetermined area of cache memory and storing the copied data in a storage area separate from the cache memory.

30. The method of Claim 29, wherein c) comprises setting an invalid bit corresponding to the predetermined area of cache memory.

31. The method of Claim 29, wherein b) comprises:

b.1) obtaining a portion of the starting address from a storage location specified in the decoded instruction;

b.2) shifting the portion of the starting address by a predetermined number of bit positions to obtain the starting address of the cache line in which data is to be invalidated.

32. The method of Claim 31, wherein in b.1) the portion of the starting address contains a plurality of most significant bits of the starting address, and wherein in b.2), the predetermined number of bit positions represent the number of least significant bits of the starting address.

33. The method of Claim 29, wherein the predetermined portion of the plurality of cache lines is a page in the cache memory.

34. The method of Claim 29, further comprising:

d) invalidating the data in the predetermined portion of the plurality of cache lines in response to receiving the single instruction, upon copying the data to the storage area.

35. A computer-readable apparatus, comprising:

a computer-readable medium that stores an instruction which when executed by a processor causes said processor to:

obtain a starting address of a predetermined area of a cache memory on which the instruction will be performed; and

invalidate data in the predetermined area of cache memory.

36. A computer-readable apparatus comprising:

a computer-readable medium that stores an instruction which when executed by a processor causes said processor to:

obtain a starting address of a predetermined area of a cache memory on which the instruction will be performed;

copy data from the predetermined area of cache memory; and

store the copied data in a storage area separate from the cache memory.

37. The apparatus of Claim 36, wherein the instruction further causes the processor to:

invalidate the data in the predetermined portion of the plurality of cache lines in response to receiving the instruction, upon copying the data to the storage area.

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